Actel®

Product Brief

IGLOO™ Low Power Flash FPGAs with Flash*Freeze™ Technology

FlashLock®

Features and Benefits

Low Power

- 5 µW Power Consumption in Flash*Freeze Mode
- 1.2 V or 1.5 V Core Voltage for Low Power
- Supports Single-Voltage System Operation
- Low Power Active Capability Enables Active FPGA Operation with Ultra-Low Power (from 25 µW)
- Flash*Freeze Technology Enables Ultra-Low Power Consumption While Maintaining FPGA Content
- Quick and Easy Way to Enter and Exit Flash*Freeze Mode Using Flash*Freeze Pin

High Capacity

- 30 k to 1 Million System Gates
- Up to 144 kbits of True Dual-Port SRAM
- Up to 300 User I/Os

Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Live At Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design When Powered Off

In-System Programming (ISP) and Security

- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption (except AGL030) via JTAG (IEEE 1532-compliant)
- FlashLock® to Secure FPGA Contents

High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

Advanced I/O

- 700 Mbps DDR, LVDS-Capable I/Os (AGL250 and above)
- 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—Up to 4 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V/2.5 V/1.8 V/1.5 V, 3.3 V PCI/3.3 V PCI-X (except AGL030), and LVCMOS 2.5 V/5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, BLVDS, and M-LVDS (AGL250 and above)
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold Sparing I/Os (AGL030 only)
- Programmable Output Slew Rate (except AGL030) and Drive Strength
- Weak Pull-Up/Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages Across the IGLOO Family

Clock Conditioning Circuit (CCC) and PLL (except AGL030)

- Six CCC Blocks, One with an Integrated PLL
- Flexible Phase-Shift, Multiply/Divide, and Delay Capabilities
- Wide Input Frequency Range (1.5 MHz to 200 MHz)

Embedded Memory

- 1 kbit of FlashROM User Nonvolatile Memory
- SRAMs and FIFOs with Variable-Aspect Ratio 4,608-Bit RAM Blocks (x1, x2, x4, x9, and x18 organizations available)
- True Dual-Port SRAM (except x18)

Table 1 • **IGLOO Product Family**

IGLOO Devices	AGL030	AGL060	AGL125	AGL250	AGL600	AGL1000
System Gates	30 k	60 k	125 k	250 k	600 k	1 M
VersaTiles (D-Flip-Flops)	768	1,536	3,072	6,144	13,824	24,576
Quiescent Current (typical) in Flash*Freeze Mode (µA)	4	8	14	28	60	102
RAM kbits (1,024 bits)	–	18	36	36	108	144
4,608 Bit Blocks	–	4	8	8	24	32
FlashROM Bits	1 k	1 k	1 k	1 k	1 k	1 k
Secure (AES) ISP	–	Yes	Yes	Yes	Yes	Yes
Integrated PLL in CCCs	–	1	1	1	1	1
VersaNet Globals[1]	6	18	18	18	18	18
I/O Banks	2	2	2	4	4	4
Maximum User I/Os	81	96	133	143	235	300
Package Pins						
CS		CS196	CS196	CS196		
QFN	QN132	QN132	QN132	QN132		
VQFP	VQ100	VQ100	VQ100	VQ100		
FBGA		FG144	FG144	FG144	FG144, FG256, FG484	FG144, FG256, FG484

Notes:

1. *Six chip (main) and three quadrant global networks are available for AGL060 and above.*
2. *For higher densities and support of additional features, refer to the* IGLOOe Flash FPGAs *datasheet.*

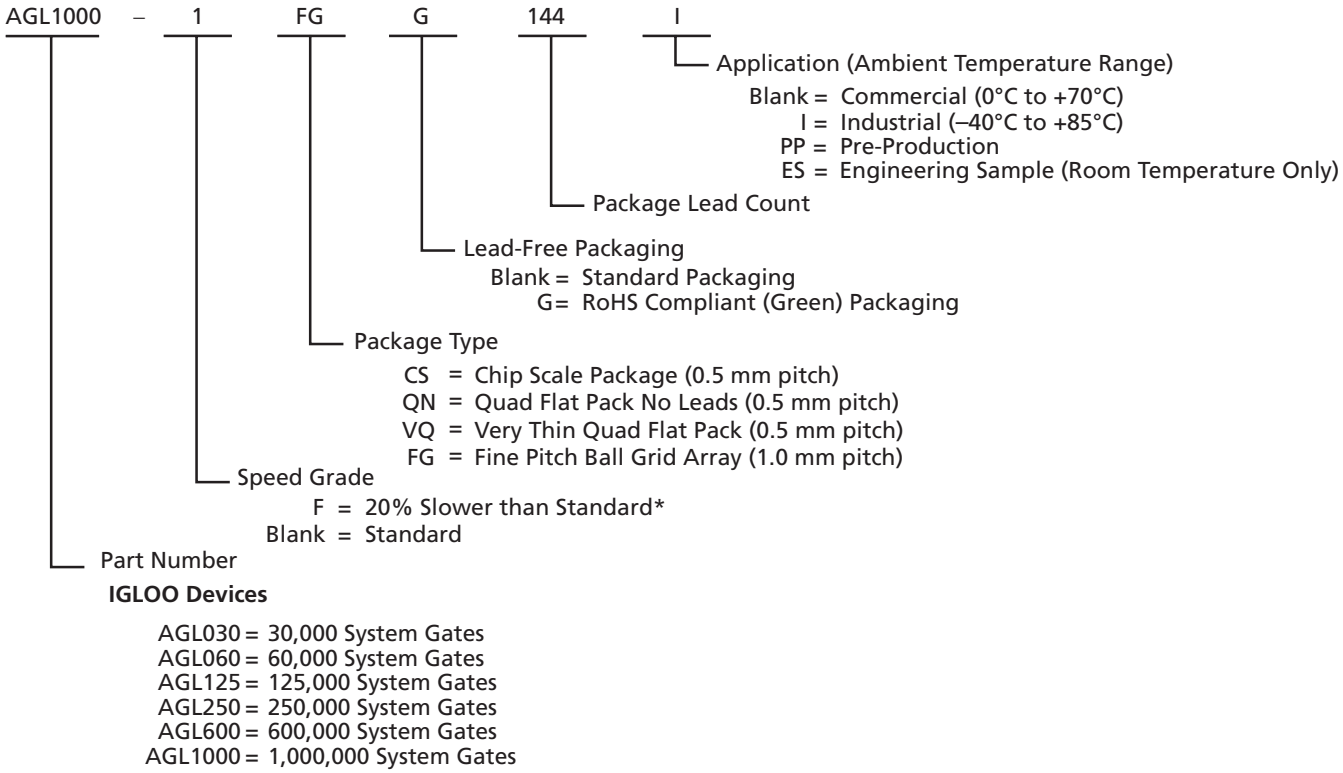
I/Os Per Package[1]

IGLOO Devices	AGL030	AGL060	AGL125	AGL250 [2]		AGL600		AGL1000	
	I/O Type								
Package (Dimensions mm)	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs
VQ100 (14x14)	77	71	71	68	13		–	–	–
QN132 (8x8)	81	80	84	87	19		–	–	–
CS196 (8x8)	–	96	133	143	30		–	–	–
FG144 (13x13)	–	96	97	97	24	97	25	97	25
FG256 (17x17)	–	–	–	–	–	177	43	177	44
FG484 (27x27)	–	–	–	–	–	235	60	300	74

Notes:

1. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
2. *For AGL250 devices, the maximum number of LVPECL pairs in east and west banks cannot exceed 15.*
3. *FG256 and FG484 are footprint-compatible packages.*
4. *When the Flash*Freeze pin is used to enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by 1.*
5. *"G" indicates RoHS compliant packages. Refer to the "IGLOO Ordering Information" on page 3 for the location of the "G" in the part number.*

IGLOO Ordering Information



IGLOO Devices

AGL030 = 30,000 System Gates
AGL060 = 60,000 System Gates
AGL125 = 125,000 System Gates
AGL250 = 250,000 System Gates
AGL600 = 600,000 System Gates
AGL1000 = 1,000,000 System Gates

Note: **The characteristics provided for –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in commercial temperature range.*

Temperature Grade Offerings

Package	AGL030	AGL060	AGL125	AGL250	AGL600	AGL1000
VQ100	C, I	C, I	C, I	C, I	–	–
QN132	C, I	C, I	C, I	C, I	–	–
CS196	–	C, I	C, I	C, I	–	–
FG144	–	C, I	C, I	C, I	C, I	C, I
FG256	–	–	–	–	C, I	C, I
FG484	–	–	–	–	C, I	C, I

Notes:

1. *C = Commercial temperature range: 0°C to 70°C ambient*
2. *I = Industrial temperature range: –40°C to 85°C ambient*

Speed Grade and Temperature Grade Matrix

Temperature Grade	–F [1]	Std.
C [2]	✓	✓
I [3]	–	✓

Notes:

1. *The characteristics provided for –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in commercial temperature range.*
2. *C = Commercial temperature range: 0°C to 70°C ambient*
3. *I = Industrial temperature range: –40°C to 85°C ambient*

Contact your local Actel representative for device availability (http://www.actel.com/company/contact/offices/).

Introduction and Overview

General Description

The IGLOO family of Flash FPGAs, based on a 130-nm Flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Low Power Active capability (static idle) allows for ultra-low power consumption (from 25 µW) while the IGLOO device is completely functional in the system by maintaining I/O, SRAM, registers, and logic functions. This allows the IGLOO device to control the system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

The Flash*Freeze technology used in IGLOO devices allows entering and exiting an ultra-low power mode that consumes as little as 5 µW while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

Nonvolatile Flash technology gives IGLOO devices the advantage of being a secure, low power, single-chip solution that is live at power-up (LAPU). IGLOO is reprogrammable and offers time to market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM memory storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The AGL030 device has no PLL or RAM support. IGLOO devices have up to 1 million system gates, supported with up to 144 kbits of true dual-port SRAM, and up to 288 user I/Os.

Flash*Freeze Technology

The IGLOO device offers unique Flash*Freeze technology that allows the IGLOO device to enter and exit an ultra-low power mode. IGLOO devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. The Flash*Freeze technology is combined with in-system programmability, which allows users to quickly and easily upgrade and update the design in the final stages of manufacturing or in the field. The ability of IGLOO to support 1.2 V core voltage allows further reduction of power consumption, thus achieving the lowest total system power.

Flash*Freeze technology allows the user to keep all power supplies, I/Os, and clocks connected to the device in normal operation. When the IGLOO device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

This low power feature, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high pin-count packages, makes IGLOO devices the best fit for portable electronics.

Flash Advantages

Low Power

Flash-based IGLOO devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO devices also have low dynamic power consumption to further maximize power savings, which is also reduced by the use of 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, makes the IGLOO device the lowest total system power offered by any FPGA.

Security

The nonvolatile, Flash-based IGLOO devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile Flash programming can offer.

IGLOO devices utilize a 128-bit Flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in the IGLOO devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000, and replaces the 1977 DES standard. IGLOO devices have a built-in AES

decryption engine and a Flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed IGLOO device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of the IGLOO family. The Flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOO family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. An IGLOO device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store the configuration information in on-chip Flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, Flash-based IGLOO FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load the device configuration data. This reduces bill-of-materials costs and printed circuit board (PCB) area, and increases security and system reliability.

Live at Power-Up

The Actel Flash-based IGLOO devices support Level 0 of the live at power-up (LAPU) classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of Flash-based IGLOO devices greatly simplifies total system design and reduces total system cost, often eliminating the need for complex programmable logic devices (CPLDs) and clock generation PLLs that are used for these purposes in a system. In addition, glitches and brownouts in system power will not corrupt the IGLOO device's Flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO devices simplify total system design, and reduce cost and design risk, while increasing system reliability and improving system initialization time.

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, Flash-based IGLOO devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/ communications, computing, and avionics markets.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO Flash-based FPGAs. Once it is programmed, the Flash cell configuration element of IGLOO FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOO family offers many benefits, including nonvolatility and reprogrammability through an advanced Flash-based, 130-nm LVCMOS process with 7 layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant Flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

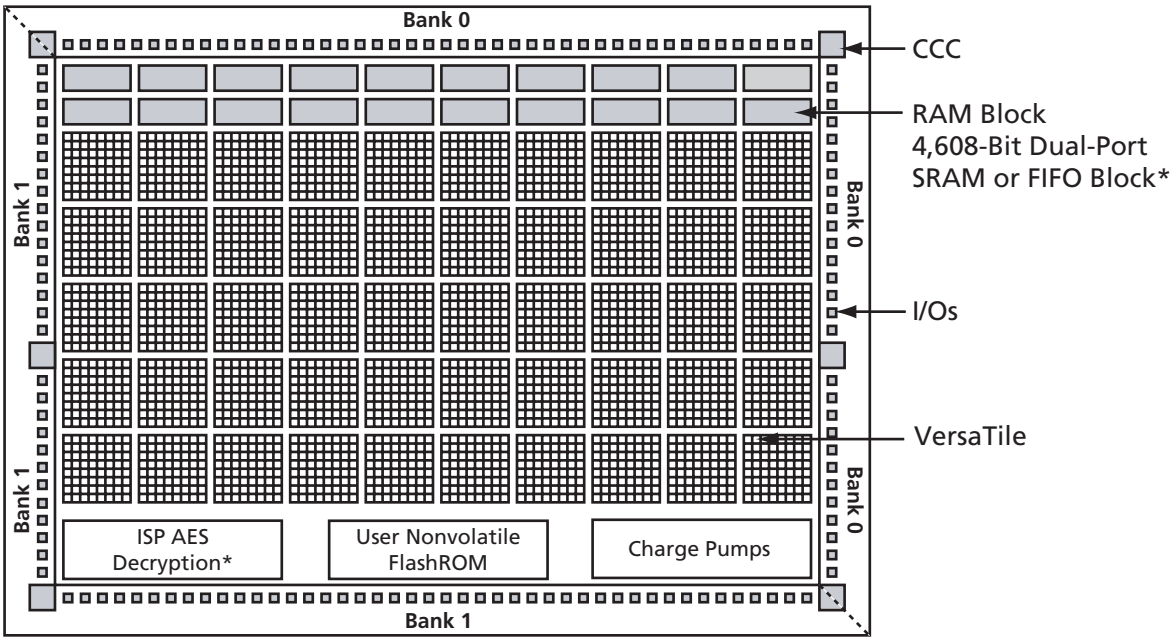
Advanced Architecture

The proprietary IGLOO architecture provides granularity comparable to standard-cell ASICs. The IGLOO device consists of five distinct and programmable architectural features (Figure 1 and Figure 2 on page 8):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM memory
- Dedicated SRAM/FIFO memory[1]
- Extensive clock conditioning circuitry (CCC) and PLLs[1]
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function or as a D-flip-flop (with or without enable), or as a latch, by programming the appropriate Flash switch interconnections. The versatility of the IGLOO core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC® families of third generation architecture Flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of the IGLOO devices via an IEEE 1532 JTAG interface.



Note: **Not supported by AGL030*

Figure 1 • **Device Architecture Overview with Two I/O Banks (AGL030, AGL060, and AGL125)**

1. *The AGL030 does not support PLL and SRAM.*

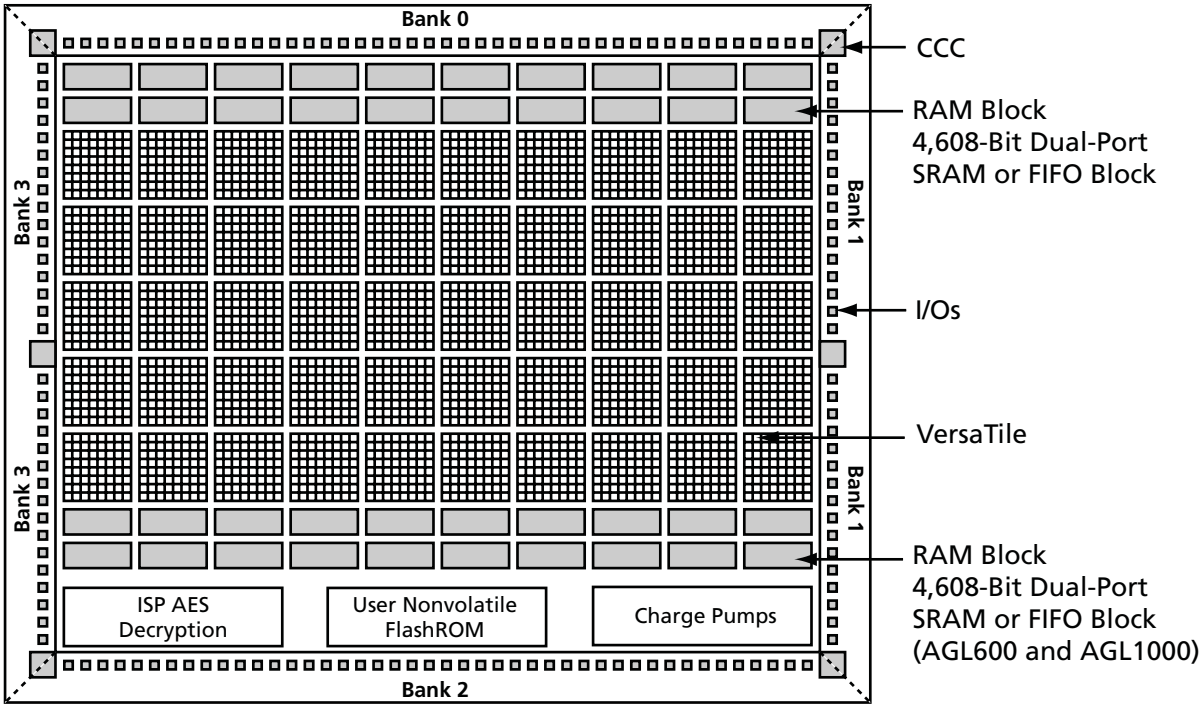


Figure 2 • **Device Architecture Overview with Four I/O Banks (AGL250, AGL600, and AGL1000)**

Flash*Freeze Technology

The IGLOO device has an ultra-low power static mode that retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology allows the user to quickly enter and exit Flash*Freeze mode within 1 µs by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and states. No power is consumed by the I/Os, clocks, JTAG pins, or PLL, and the device consumes as little as 5 µW in this mode.

Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active high) can be routed internally to the core to allow the user's logic to decide if it is safe to transition to this mode. It is also possible to use the Flash*Freeze pin as a regular I/O if the Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low power static (as low as 25 µW) and dynamic capabilities of the IGLOO device. Refer to Figure 3 for an illustration of entering/exiting Flash*Freeze mode. For more information on how to use the Flash*Freeze mode, refer to the *Low Power Modes in Actel IGLOO FPGAs* application note.

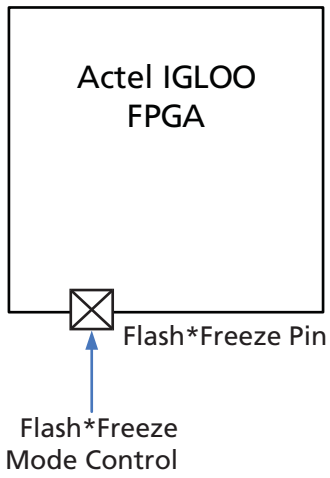


Figure 3 • **IGLOO Flash*Freeze Mode**

VersaTiles

The IGLOO core consists of VersaTiles, which have been enhanced beyond the ProASIC[PLUS]® core tiles. The IGLOO VersaTile supports the following:

- All three-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 4 for VersaTile configurations.

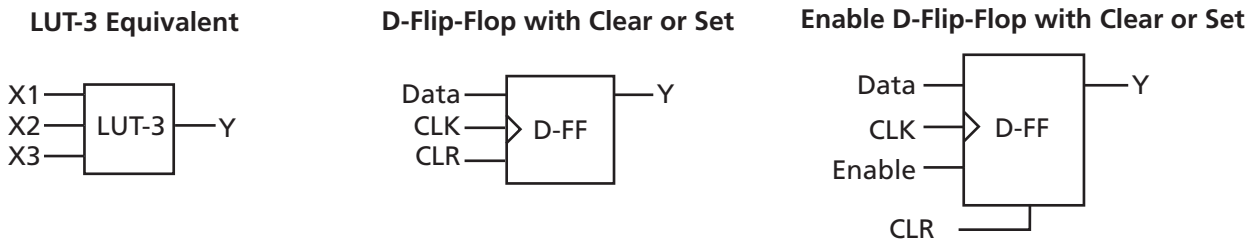


Figure 4 • **VersaTile Configurations**

User Nonvolatile FlashROM

Actel IGLOO devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the AGL030 device), such as security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface, and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel IGLOO development software solutions, Libero® Integrated Design Environment (IDE) and Designer, have extensive support for the FlashROM memory. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

IGLOO devices (except in the AGL030 device) have embedded SRAM blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256x18, 512x9, 1kx4, 2kx2, and 4kx1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in the AGL030 device).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost-Empty (AEMPTY) and Almost-Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and Clock Conditioning Circuitry (CCC)

IGLOO devices provide designers with very flexible clock conditioning capabilities. Each member of the IGLOO family contains six CCCs. One CCC (center west side) has a PLL. The AGL030 does not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several I/O inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 200 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 200 MHz
- Two programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time = 200 µs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × (200 MHz / f_{OUT_CCC}) (for PLL only)

Global Clocking

IGLOO devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.

I/Os with Advanced I/O Standards

The IGLOO family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). IGLOO FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, BLVDS, and M-LVDS I/Os for point-to-point communications

IGLOO banks for the AGL250 device and above support LVPECL, LVDS, BLVDS and M-LVDS. BLVDS and M-LVDS can support up to 20 loads.

Quiescent Supply Current

Table 2 • **Quiescent Supply Current (I_{DD}), Flash*Freeze Mode†**

	Core Voltage	AGL030	AGL060	AGL125	AGL250	AGL600	AGL1000	Units
Typical (25°C)	1.2 V	4	8	14	28	60	102	µA
	1.5 V	6	10	18	34	72	127	µA

Note: *†I_{DD} includes V_{CC}, V_{PUMP}, V_{CCI}, VMV, and I/O static currents in worst case conditions.*

Table 3 • **Quiescent Supply Current (I_{DD}), Sleep Mode (V_{CC} = 0 V)†**

	AGL030	AGL060	AGL125	AGL250	AGL600	AGL1000	Units
V_{CCI} = 1.5 V (all banks) Typical (25°C)	5	5	5	9	9	9	µA
V_{CCI} = 1.8 V (all banks) Typical (25°C)	5	5	5	11	11	11	µA
V_{CCI} = 2.5 V (all banks) Typical (25°C)	8	8	8	15	15	15	µA
V_{CCI} = 3.3 V (all banks) Typical (25°C)	10	10	10	20	20	20	µA

Note: *†I_{DD} includes V_{CC}, V_{PUMP}, V_{CCI}, and VMV currents. Values do not include I/O static contribution.*

Table 4 • **Quiescent Supply Current (I_{DD}), Shutdown Mode (V_{CC}, V_{CCI} = 0 V)†**

	Core Voltage	AGL030	Units
Typical (25°C)	1.2 V / 1.5 V	0	µA

Note: *†I_{DD} includes V_{CC}, V_{PUMP}, V_{CCI}, and VMV currents. Values do not include I/O static contribution.*

Table 5 • **Quiescent Supply Current, No Flash*Freeze Mode[1]**

	Core Voltage	AGL030	AGL060	AGL125	AGL250	AGL600	AGL1000	Units
I_{CCA} Current[2]								
Typical (25°C)	1.2V	14	18	24	38	70	112	µA
	1.5V	16	20	28	44	82	137	µA
I_{CCI} or I_{JTAG} Current[3, 4]								
3.3 V Typical (25°C)	1.2 V / 1.5 V	5	5	5	5	5	5	µA
2.5 V Typical (25°C)	1.2 V / 1.5 V	4	4	4	4	4	4	µA
1.8 V Typical (25°C)	1.2 V / 1.5 V	3	3	3	3	3	3	µA
1.5 V Typical (25°C)	1.2 V / 1.5 V	2	2	2	2	2	2	µA

Notes:

1. *To calculate total device I_{DD}, multiply the number of banks used in I_{CCI} and add I_{CCA} contribution.*
2. *Includes V_{CC} and V_{PUMP} currents*
3. *Per V_{CCI} or V_{JTAG} bank*
4. *Values do not include I/O static contribution.*

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Web-only." The definition of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this datasheet are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

www.actel.com

Actel Corporation
2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.
River Court, Meadows Business Park
Station Approach, Blackwater
Camberley, Surrey GU17 9AB
United Kingdom
Phone +44 (0) 1276 609 300
Fax +44 (0) 1276 607 540

Actel Japan
EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668
www.jp.actel.com

Actel Hong Kong
Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488
www.actel.com.cn

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